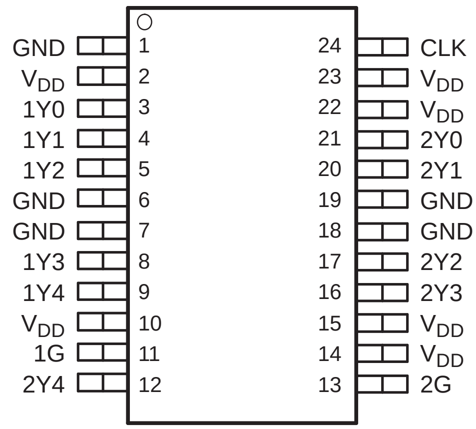
2.5-V TO 3.3-V HIGH-PERFORMANCE CLOCK BUFFER

FEATURES

- **High-Performance 1:10 Clock Driver**
- **Pin-to-Pin Skew < 100 ps at V_{DD} 3.3 V**
- **V_{DD} Range = 2.3 V to 3.6 V**
- **Input Clock Up To 200 MHz (See Figure 7)**
- **Operating Temperature Range –40°C to 85°C**
- **Output Enable Glitch Suppression**
- **Distributes One Clock Input to Two Banks of Five Outputs**
- **Packaged in 24-Pin TSSOP**
- **Pin-to-Pin Compatible to the CDCVF2310, Except the R = 22-Ω Series Damping Resistors at Yn**

PW PACKAGE
(TOP VIEW)



APPLICATIONS

- **General-Purpose Applications**

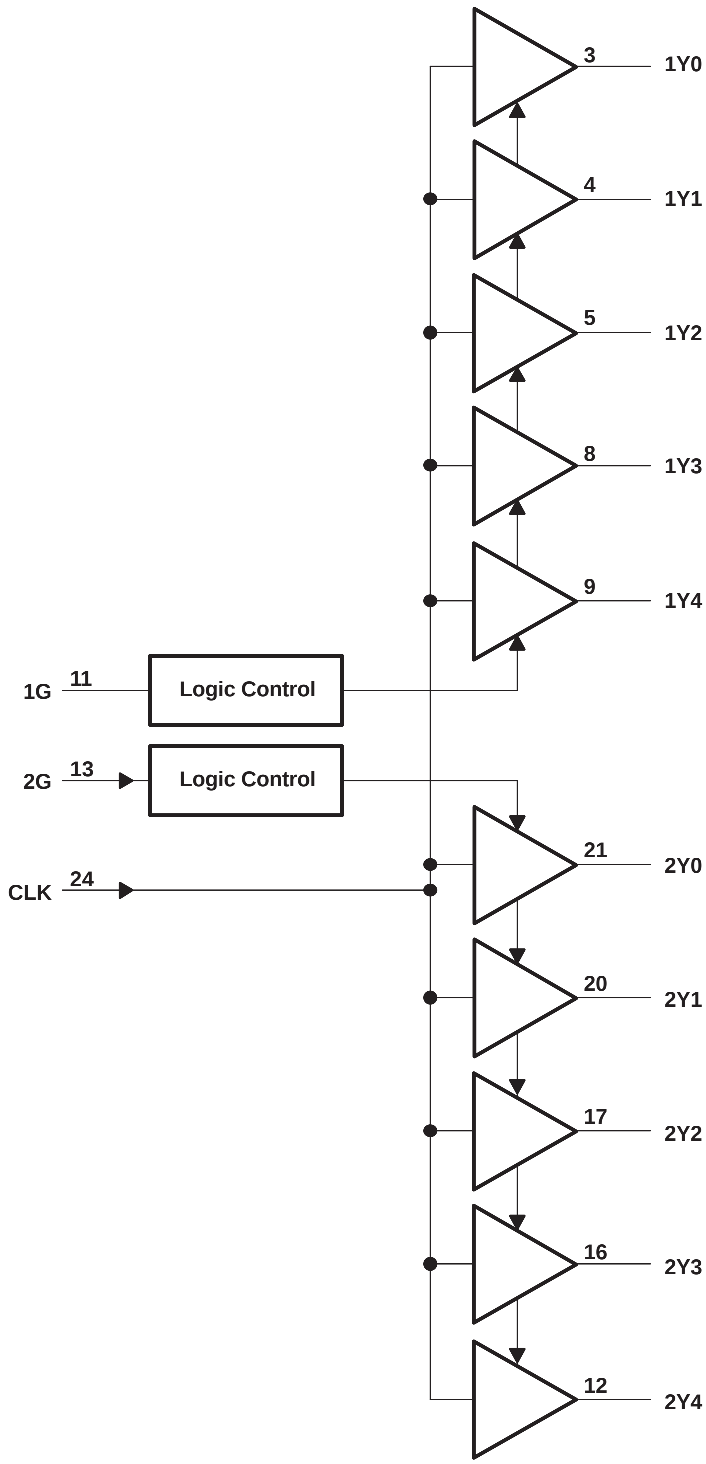
DESCRIPTION

The CDCVF310 is a high-performance, low-skew clock buffer that operates up to 200 MHz. Two banks of five outputs each provide low-skew copies of CLK. After power up, the default state of the outputs is low regardless of the state of the control pins. For normal operation, the outputs of bank 1Y[0:4] or 2Y[0:4] can be placed in a low state when the control pins (1G or 2G, respectively) are held low and a negative clock edge is detected on the CLK input. The outputs of bank 1Y[0:4] or 2Y[0:4] can be switched into the buffer mode when the control pins (1G and 2G) are held high and a negative clock edge is detected on the CLK input. The device operates in a 2.5-V and 3.3-V environment. The built-in output enable glitch suppression ensures a synchronized output enable sequence to distribute full period clock signals.

The CDCVF310 is characterized for operation from –40C to 85C.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTIONAL BLOCK DIAGRAM



FUNCTION TABLE

INPUT			OUTPUT	
1G	**2G**	**CLK**	**1Y[0:4]**	**2Y[0:4]**
L	L	↓	L	L
H	L	↓	CLK(1)	L
L	H	↓	L	CLK(1)
H	H	↓	CLK(1)	CLK(1)

(1) After detecting one negative edge on the CLK input, the output follows the input CLK if the control pin is held high.

Terminal Functions

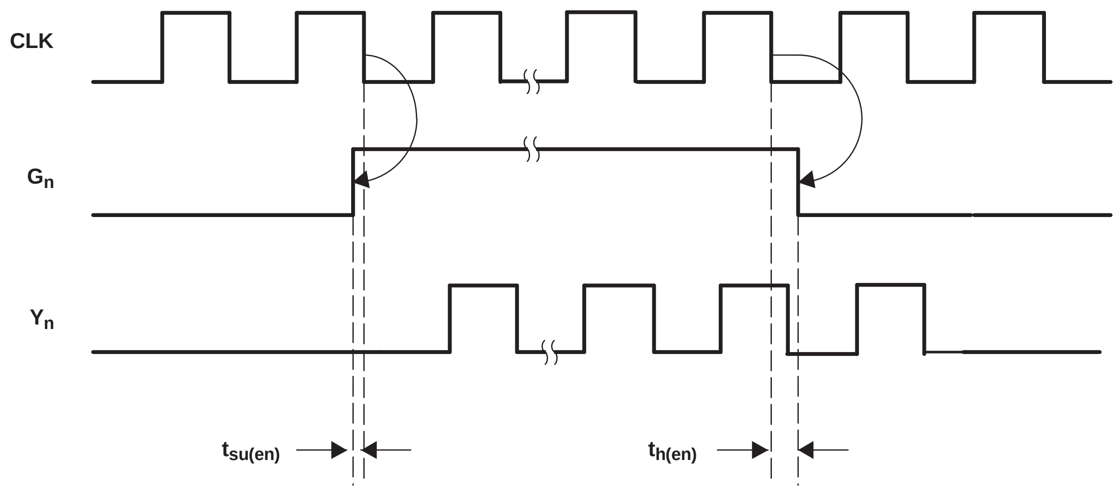
TERMINAL		I/O	DESCRIPTION
NAME	**NO.**		
1G	11	I	Output enable control for 1Y[0:4] outputs. This output enable is active-high, meaning the 1Y[0:4] clock outputs follow the input clock (CLK) if this pin is logic high.
2G	13	I	Output enable control for 2Y[0:4] outputs. This output enable is active-high, meaning the 2Y[0:4] clock outputs follow the input clock (CLK) if this pin is logic high.
1Y[0:4]	3, 4, 5, 8, 9	O	Buffered output clocks
2Y[0:4]	21, 20, 17, 16, 12	O	Buffered output clocks
CLK	24	I	Input reference frequency
GND	1, 6, 7, 18, 19		Ground
V_{DD}	2, 10, 14, 15, 22, 23		DC power supply, 2.3 V – 3.6 V

DETAILED DESCRIPTION

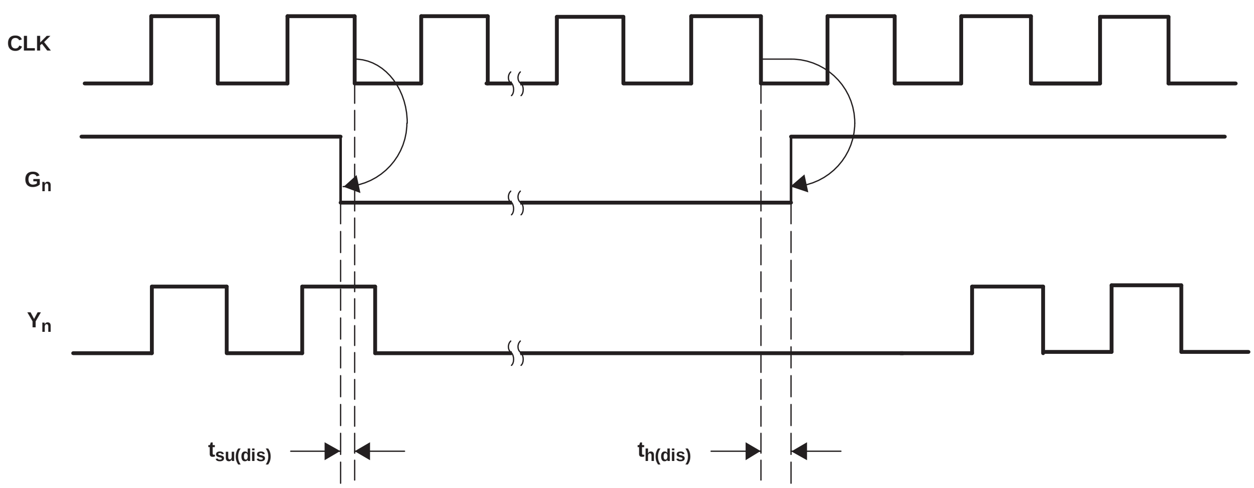
Output Enable Glitch Suppression Circuit

The purpose of the glitch suppression circuitry is to ensure the output enable sequence is synchronized with the clock input such that the output buffer is enabled or disabled on the next full period of the input clock (negative edge triggered by the input clock) (see Figure 1).

The G input must fulfill the timing requirements (t_{su}, t_h) according to the *Switching Characteristics* table for predictable operation.



a) Enable Mode



b) Disable Mode

Figure 1. Enable and Disable Mode Relative to CLK↓

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

Supply voltage range, V_{DD}		–0.5 V to 4.6 V
Input voltage range, V_I (2) (3)		–0.5 V to V_{DD} + 0.5 V
Output voltage range, V_O (2) (3)		–0.5 V to V_{DD} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I> V_{DD})		±50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD})		±50 mA
Continuous total output current, I_O (V_O = 0 to V_{DD})		±50 mA
Package thermal impedance, θ_{JA} (4): PW package		88°C/W, high K
		120°C/W, low K
Storage temperature range T_{stg}		–65°C to 150°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) This value is limited to 4.6 V maximum.
(4) The package thermal impedance is calculated in accordance with JESD 51.

RECOMMENDED OPERATING CONDITIONS (1)

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		2.3	2.5		V
			3.3	3.6	
Low-level input voltage, V_{IL}	V_{DD} = 3 V to 3.6 V			0.8	V
	V_{DD} = 2.3 V to 2.7 V			0.7	
High-level input voltage, V_{IH}	V_{DD} = 3 V to 3.6 V	2			V
	V_{DD} = 2.3 V to 2.7 V	1.7			
Input voltage, V_I		0		V_{DD}	V
High-level output current, I_{OH}	V_{DD} = 3 V to 3.6 V			–12	mA
	V_{DD} = 2.3 V to 2.7 V			–6	
Low-level output current, I_{OL}	V_{DD} = 3 V to 3.6 V			12	mA
	V_{DD} = 2.3 V to 2.7 V			6	
Operating free-air temperature, T_A		–40		85	°C

(1) Unused inputs must be held high or low to prevent them from floating.

TIMING REQUIREMENTS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clk}	Clock frequency	V_{DD} = 2.3 V to 3.6 V, See Figure 7	0		200	MHz

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IK}	Input voltage	V_{DD} = 3 V,	I_I = –18 mA			–1.2	V
I_I	Input current	V_I = 0 V or V_{DD}				±5	μA
I_{DD} (2)	Static device current	CLK = 0 V or V_{DD} = 3.6 V,	I_O = 0 mA			80	μA
C_I	Input capacitance	V_{DD} = 2.3 V to 3.6 V,	V_I = 0 V or V_{DD}		2.5		pF
C_O	Output capacitance	V_{DD} = 2.3 V to 3.6 V,	V_I = 0 V or V_{DD}		2.6		pF
C_{PD}	Power dissipation (3)	V_{DD} = 2.3 V to 3.6 V,	V_I= 0 V or V_{DD}			32	pF

(1) All typical values are with respect to nominal V_{DD}.
(2) For dynamic I_{DD} over Frequency see Figure 6.
(3) This is the formula for the power dissipation calculation.

$$P\_tot = P\_stat + P\_Dyn + P\_Load[W]$$
$$P\_stat = V_{DD} \times I_{DD} [W]$$
$$P\_Dyn = C\_PD \times V_{DD} \times V_{DD} \times f [W]$$
$$P\_Load = C\_Load \times V_{DD} \times V_{DD} \times f \times n [W]$$
$$n = \text{Number of switching output pins}$$

V_{DD} = 3.3 V ±0.3 V

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{OH}	High-level output voltage	V_{DD} = min to max,	I_{OH} = –100 μA	V_{DD} - 0.2			V
		V_{DD} = 3 V	I_{OH} = –12 mA	2.1			
			I_{OH} = –6 mA	2.4			
V_{OL}	Low-level output voltage	V_{DD} = min to max,	I_{OL} = 100 μA			0.2	V
		V_{DD} = 3 V	I_{OL} = 12 mA			0.4	
			I_{OL} = 6 mA			0.3	
I_{OH}	High-level output current	V_{DD} = 3 V,	V_O = 1 V	–37			mA
		V_{DD} = 3.3 V,	V_O = 1.65 V		–57		
		V_{DD} = 3.6 V,	V_O = 3.135 V			–38	
I_{OL}	Low-level output current	V_{DD} = 3 V,	V_O = 1.95 V	37			mA
		V_{DD} = 3.3 V,	V_O = 1.65 V		57		
		V_{DD} = 3.6 V,	V_O = 0.4 V			38	

(1) All typical values are with respect to nominal V_{DD}.

V_{DD} = 2.5 V ±0.2 V

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{OH}	High-level output voltage	V_{DD} = min to max,	I_{OH} = –100 A	V_{DD} - 0.2			V
		V_{DD} = 2.3 V	I_{OH} = –6 mA	1.8			
V_{OL}	Low-level output voltage	V_{DD} = min to max,	I_{OL} = 100 A			0.2	V
		V_{DD} = 2.3 V	I_{OL} = 6 mA			0.4	
I_{OH}	High-level output current	V_{DD} = 2.3 V,	V_O = 1 V	–20			mA
		V_{DD} = 2.5 V,	V_O = 1.25 V		–36		
		V_{DD} = 2.7 V,	V_O = 2.375 V			–25	
I_{OL}	Low-level output current	V_{DD} = 2.3 V,	V_O = 1.2 V	20			mA
		V_{DD} = 2.5 V,	V_O = 1.25 V		36		
		V_{DD} = 2.7 V,	V_O = 0.3 V			25	

(1) All typical values are with respect to nominal V_{DD}.

JITTER CHARACTERISTICS

Characterized using CDCVF310 Performance EVM when V_{DD}=3.3 V. Outputs not under test are terminated to 50 Ω.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{jitter}	Additive phase jitter from input to output 1Y0	12 kHz to 5 MHz, f_{out} = 30.72 MHz		47		fs rms
		12 kHz to 20 MHz, f_{out} = 125 MHz		40		

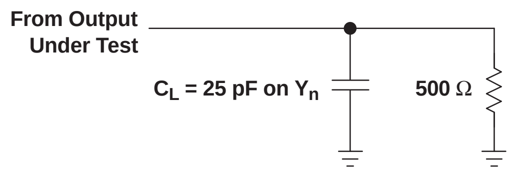
SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[(1)]	MAX	UNIT
V_{DD} = 3.3 V ±0.3 V (see Figure 2)						
t_{PLH}	CLK to Yn	f = 0 MHz to 200 MHz	1		2.8	ns
t_{PHL}			1		2.8	
$t_{sk(o)}$	Output skew (Ym to Yn) [(2)] (see Figure 4)			100	150	ps
$t_{sk(p)}$	Pulse skew (see Figure 5)				250	ps
$t_{sk(pp)}$	Part-to-part skew				350	ps
t_r	Rise time	V_O = 0.4 V to 2 V	1.3		2.7	V/ns
t_f	Fall time	V_O = 2 V to 0.4 V	1.3		2.7	V/ns
$t_{su(en)}$	Enable setup time, G_high before CLK ↓		0.1			ns
$t_{su(dis)}$	Disable setup time, G_low before CLK ↓		0.1			ns
$t_{h(en)}$	Enable hold time, G_high after CLK ↓		0.4			ns
$t_{h(dis)}$	Disable hold time, G_low after CLK ↓		0.4			ns
V_{DD} = 2.5 V ±0.2 V (see Figure 2)						
t_{PLH}	CLK to Yn	f = 0 MHz to 200 MHz	1.3		4	ns
t_{PHL}			1.3		4	
$t_{sk(o)}$	Output skew (Ym to Yn) [(2)] (see Figure 4)			150	230	ps
$t_{sk(p)}$	Pulse skew (see Figure 5)				280	ps
$t_{sk(pp)}$	Part-to-part skew				400	ps
t_r	Rise time	V_O = 0.4 V to 1.7 V	0.5		1.6	V/ns
t_f	Fall time	V_O = 1.7 V to 0.4 V	0.5		1.6	V/ns
$t_{su(en)}$	Enable setup time, G_high before CLK ↓		0.1			ns
$t_{su(dis)}$	Disable setup time, G_low before CLK ↓		0.1			ns
$t_{h(en)}$	Enable hold time, G_high after CLK ↓		0.4			ns
$t_{h(dis)}$	Disable hold time, G_low after CLK ↓		0.4			ns

(1) All typical values are with respect to nominal V_{DD}.
(2) The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.

PARAMETER MEASUREMENT INFORMATION



A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: Clock Frequency ≤ 200 MHz, Z_O = 50 Ω,
t_r < 1.2 ns, t_f < 1.2 ns.

Figure 2. Test Load Circuit

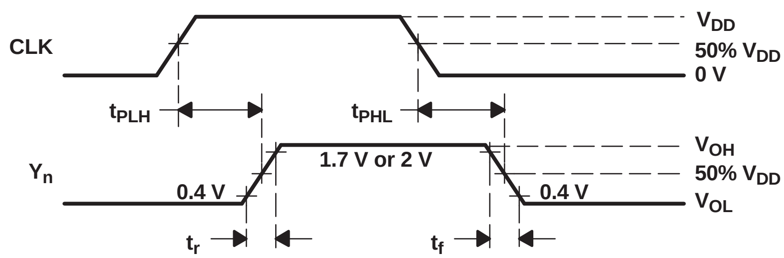


Figure 3. Voltage Waveforms Propagation Delay Times

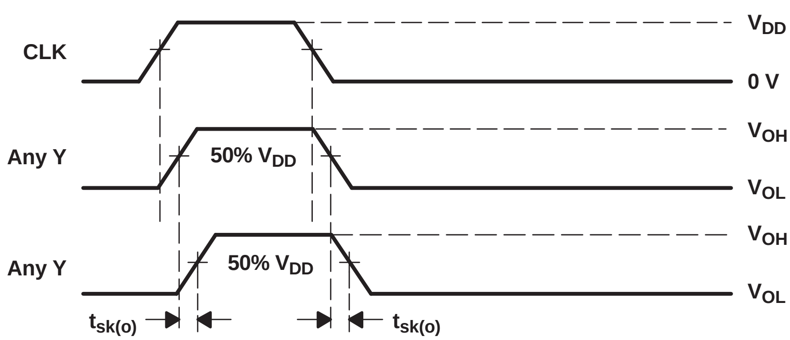
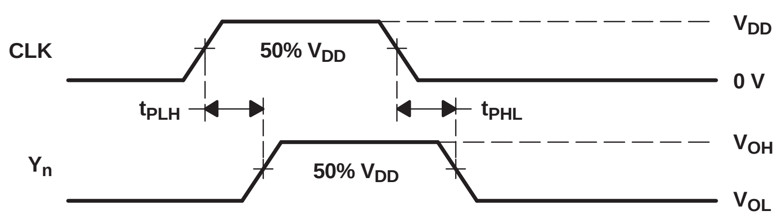


Figure 4. Output Skew



NOTE: $t_{sk(p)} = | t_{PLH} - t_{PHL} |$

Figure 5. Pulse Skew

DYNAMIC SUPPLY CURRENT
vs
CLOCK FREQUENCY

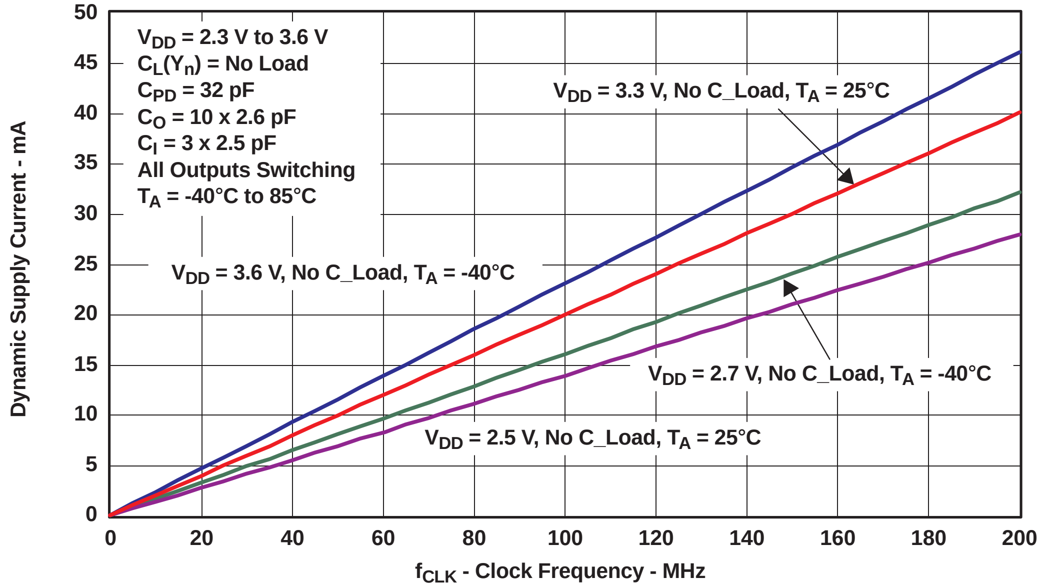


Figure 6.

C_LOAD(max) PER OUTPUT PIN Yn
vs
CLOCK FREQUENCY

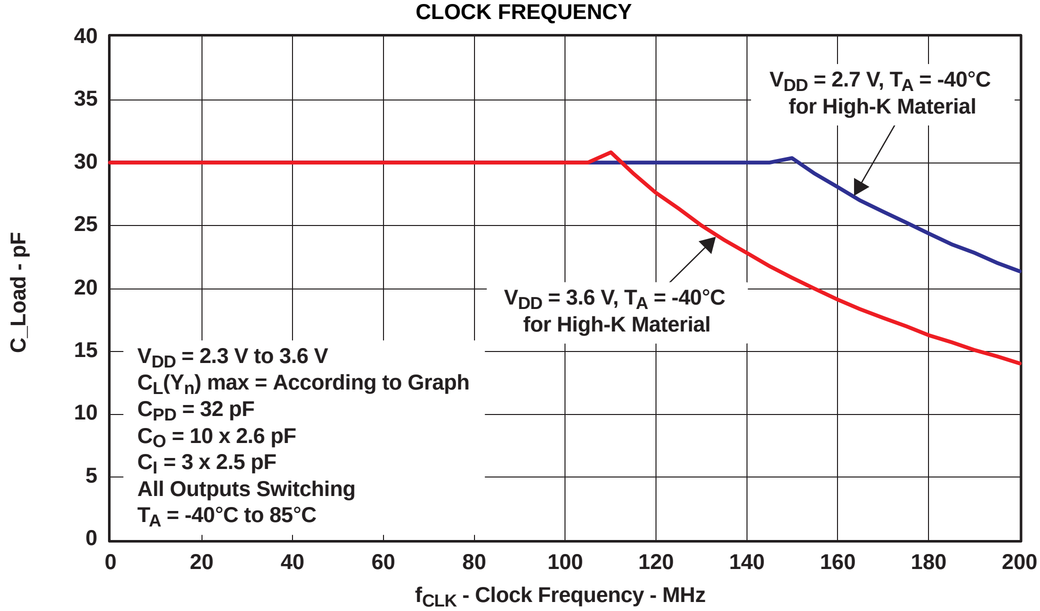


Figure 7.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CDCVF310PW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKV310	Samples
CDCVF310PWG4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKV310	Samples
CDCVF310PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKV310	Samples
CDCVF310PWRG4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKV310	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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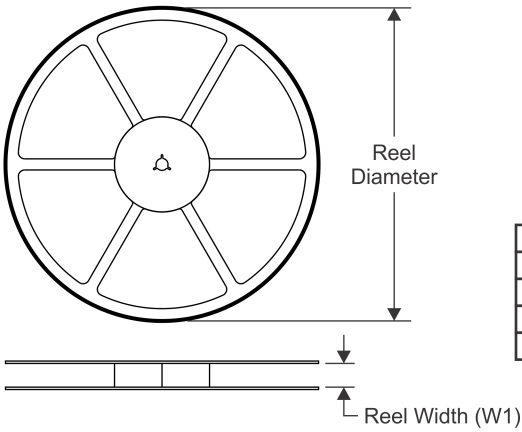
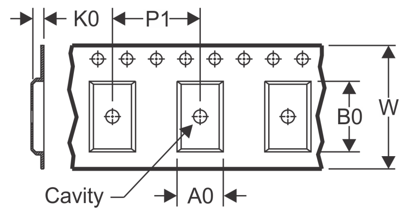
TAPE AND REEL INFORMATION

REEL DIMENSIONS

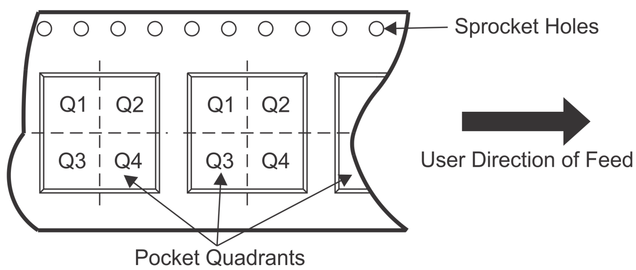


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

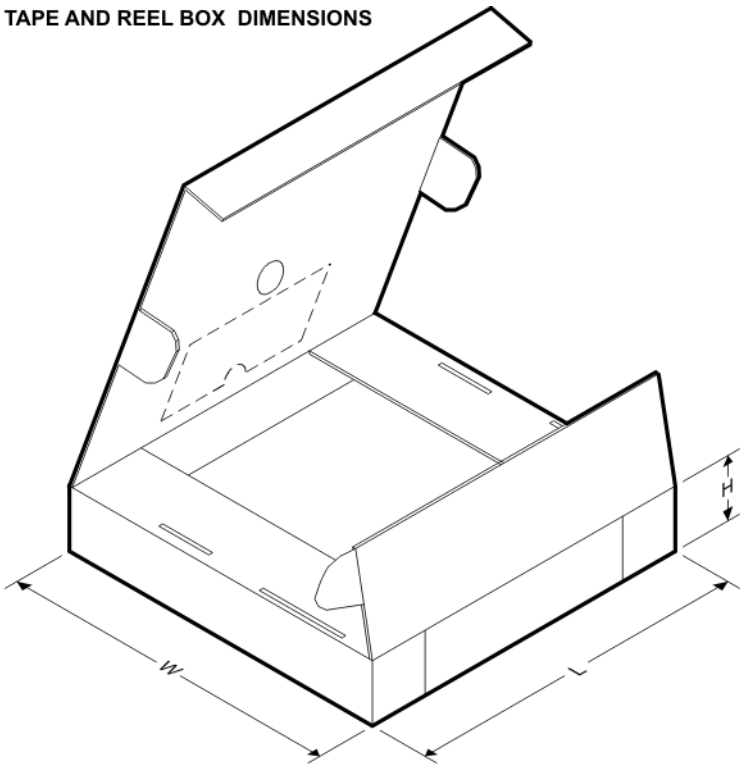
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCVF310PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

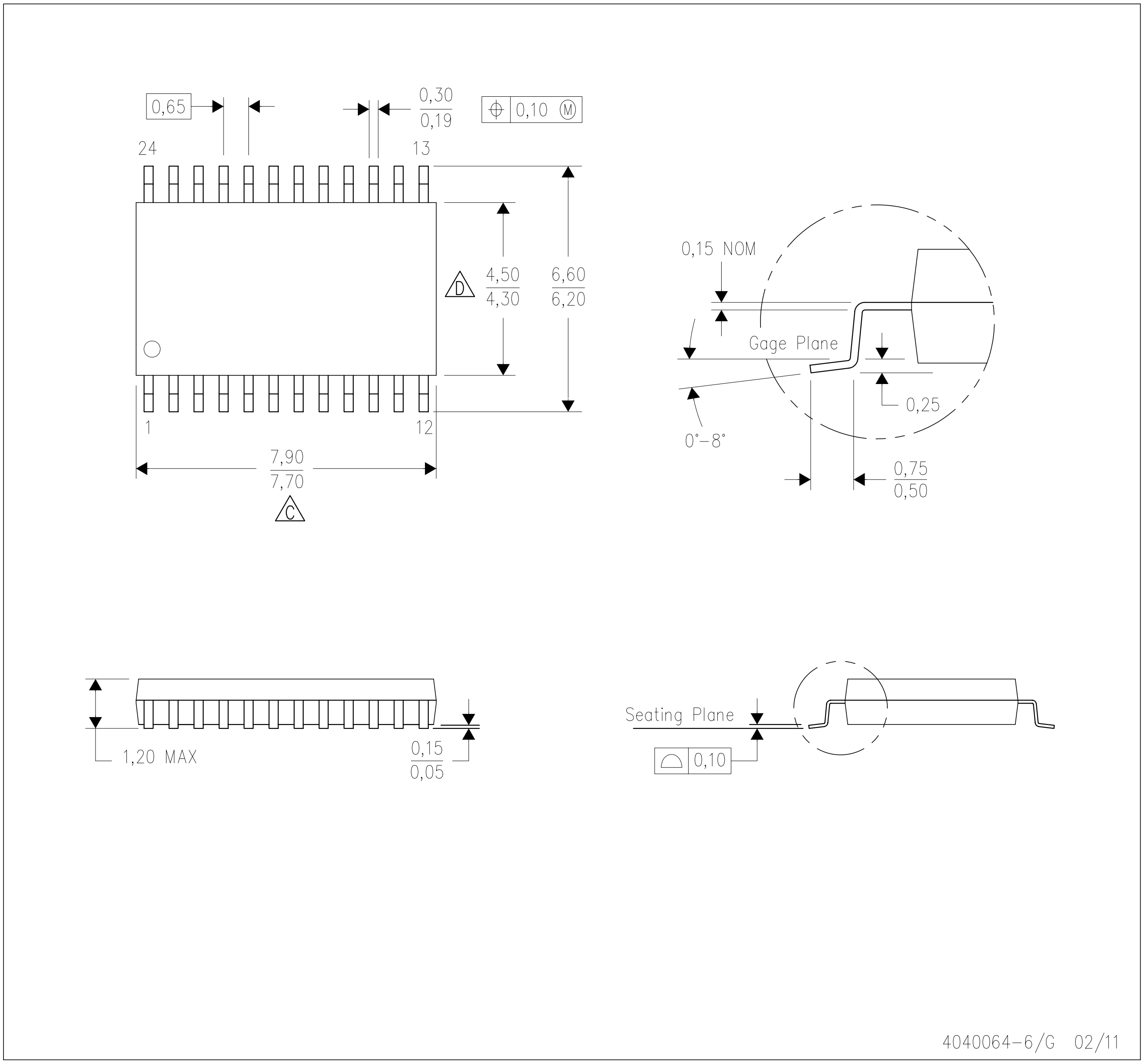
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

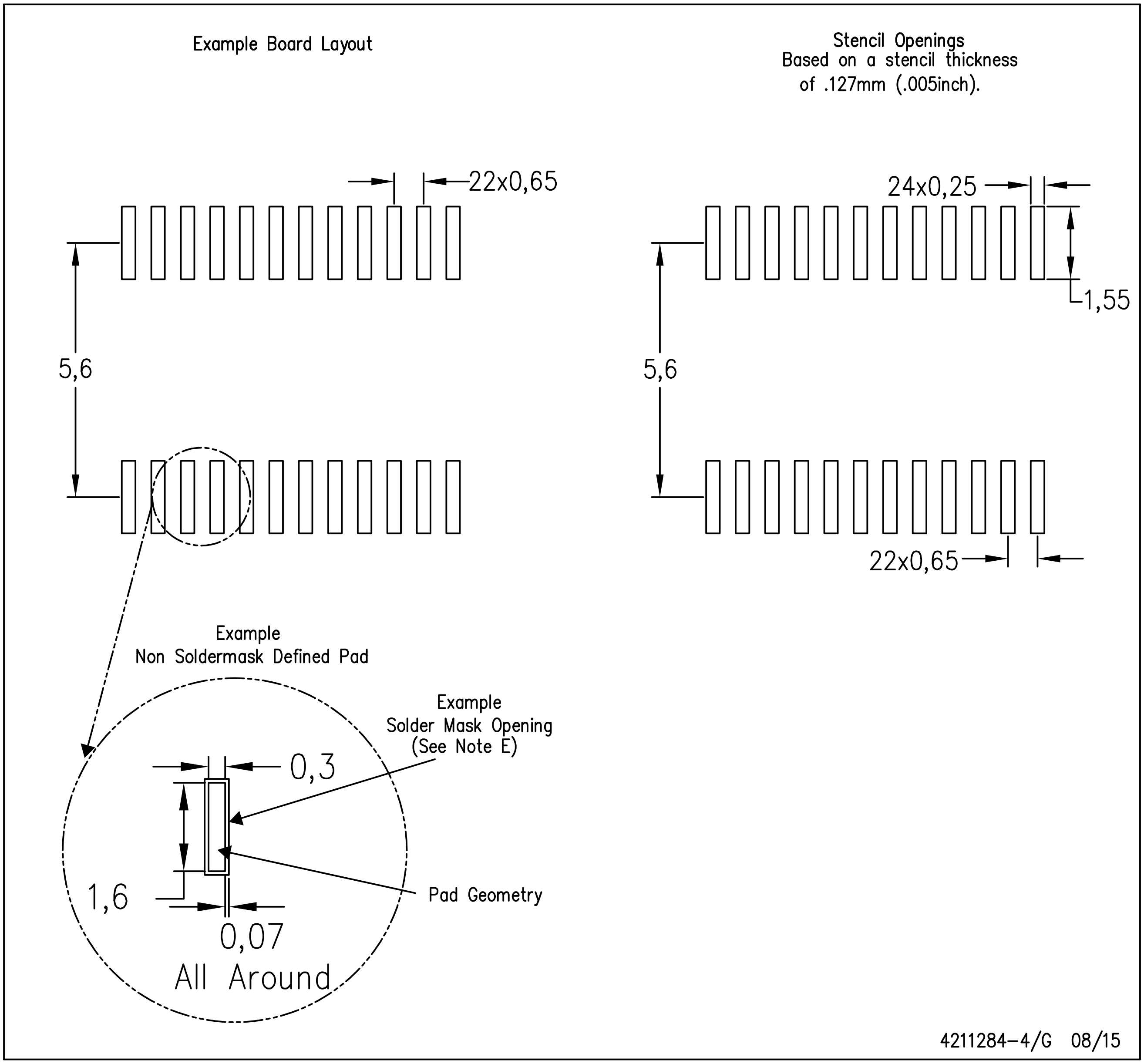
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCVF310PWR	TSSOP	PW	24	2000	367.0	367.0	38.0

PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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